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TW459242 Biblio

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Method for decreasing power consumption of semiconductor memory circuit and its semiconductor memory circuit

Patent Number: TW459242
Publication date: 2001-10-11

Inventor(s): JUNG BING-WEN (TW)
Applicant(s): MEGAWIN TECHNOLOGY CO LTD (TW)

Requested Patent: TW459242
Application Number: TW20000100396 20000112
Priority Number(s): TW20000100396 20000112
IPC Classification: G11C5/14
EC Classification:
Equivalents:

Abstract

The present invention relates to a kind of method for decreasing power consumption of semiconductor memory circuit and its circuit. When data is read out from the semiconductor memory, once the read-out address is sent to the address line, the word line is started up. And, data in the memory cell array is sent to a sensing amplifier from the bit line and is outputted. On the contrary, when data is written in, once the write-in address is sent to the address line, the same word line is started up and data to be written in is written into the memory cell array from the bit line. For the method of decreasing power consumption, when the read-out action is performed, the sensing amplifier is closed after the read-out address is sent to the address line for a predetermined time; and, when performing the write-in action, the word line is closed after the write-in address is sent to the address line for a predetermined time. Therefore, the main feature of this invention is that the time parameter is automatically predetermined to evaluate the required time for completing the action of read-out or write-in so as to decrease the unnecessary power consumption.

91136565 附件

中華民國專利公報 [19] [12]

[11]公告編號：459242
[44]中華民國 90年 (2001) 10月11日
發明 全 5 頁

[51] Int.Cl [06]: G11C5/14

[54]名 稱：減低半導體記憶體電路功率消耗之方法及其半導體記憶體電路

[21]申請案號： 089100396 [22]申請日期：中華民國 89年 (2000) 01月12日

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1 2

[57]申請專利範圍：

1.一種減低半導體記憶體電路功率消耗之方法，該半導體記憶體電路包括記憶胞耦接字元線及位元線，一位址線經一解碼器耦接至該字元線，在讀出資料時，一讀出位址送進該位址線，該字元線被開啟，該記憶胞內的資料經由該位元線送至一感測放大器輸出，該減低功率消耗的方法係在該讀出位址送進該位址線經過一讀出時間後，將該感測放大器關閉，其中該讀出時間係估算自該讀出位址送進該位址線至該感測放大器輸出資料所需要的時間。

2.如申請專利範圍第1項所述之方法，其中該感測放大器關閉後，緊接著關閉該字元線。

3.如申請專利範圍第1項所述之方法，其中係利用一計時電路耦接一控制電路控制該字元線與該感測放大器關閉，當該讀出位址送進該位址線時，該計時電路開始計時，經過該讀出時間後，即便該控制電路將該感測放大器關閉。

4.一種減低半導體記憶體電路功率消耗之方法，該半導體記憶體電路包括記憶胞耦接字元線及位元線，一位址線經一解碼器耦接至該字元線，在寫入資料時，一寫入位址送該位址線，該字元線被開啟，欲寫入的資料由該位元線寫入該記憶胞，該減低功率消耗的方法係在該寫入位址送進該位址線經過一寫入時間後，將該字元線關閉，其中該寫入時間係估算自該寫入位址送進該位址線至該欲寫入的資料寫入該記憶胞所需要的時間。

5.如申請專利範圍第4項所述之方法，其中係利用一計時電路耦接一控制電路控制該字元線關閉，當該寫入位址送進該位址線時，該計時電路開始計時，經過該寫入時間後，即使該控制

電路將該字元線關閉。

6.一種低功率消耗之半導體記憶體電路，包括：

一記憶胞，用以儲存資料；

一字元線，耦接至該記憶胞，在該半導體記憶體電路進行讀出動作時為開啟態；

一位址線，經一解碼器耦接至該字元線，在進行讀出動作時，一讀出位址送進該位址線；

一位元線，耦接該記憶胞，提供輸出該記憶胞內儲存之資料；

一感測放大器，耦接該位元線，用以將該位元線傳來的信號放大；

一計時電路，自該讀出位址送進該位址線經過一預設的讀出時間，送出一失能信號，該讀出時間係估算自該讀出位址送進該位址線至該感測放大器輸出資料所需要的時間；以及

一控制電路，耦接該計時電路與該感測放大器，該控制電路接收該失能信號，便關閉該感測放大器。

7.如申請專利範圍第6項所述之半導體記憶體電路，其中該該控制電路更耦接該字元線，該控制電路關閉該感測放大器後，緊接著關閉該字元線。

8.一種低功率消耗之半導體記憶體電路，包括：

一記憶胞，用以儲存資料；

一字元線，耦接至該記憶胞，在該半導體記憶體電路進行寫入動作時為開啟態；

一位址線，經一解碼器耦接至該字元線，在進行寫入動作時，一寫入位址送進該位址線；

一位元線，耦接該記憶胞，提供資料寫入該記憶胞；

一計時電路，自該寫入位址送進該位址線經過一預設的寫入時間，送出一失能信號，該寫入時間係估算自該寫入位址送進該位址線至該資料寫入該記憶胞所需要的時間；以及

一控制電路，耦接該計時電路與該字元線，該控制電路接收該失能信號，便關閉該字元線。

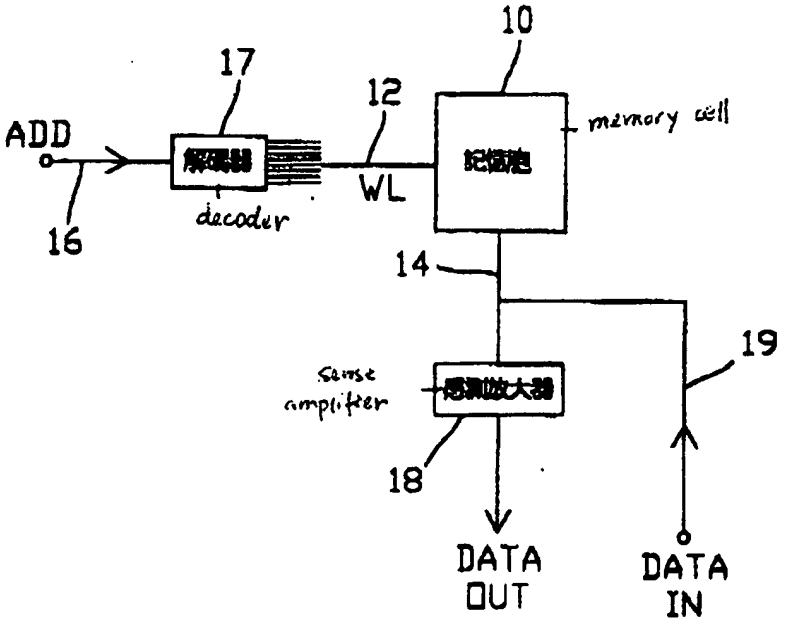
圖式簡單說明：

第一圖提供一習用半導體記憶體電路之示意圖。

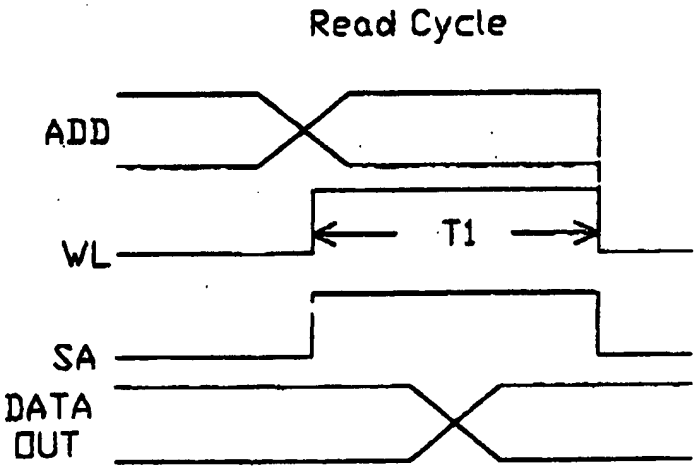
第二圖A及第二圖B提供習知技術中半導體記憶體電路在進行讀出及寫入動作時，其內部信號的時序圖。

第三圖提供一實施例，輔以說明本發明之技術特點。

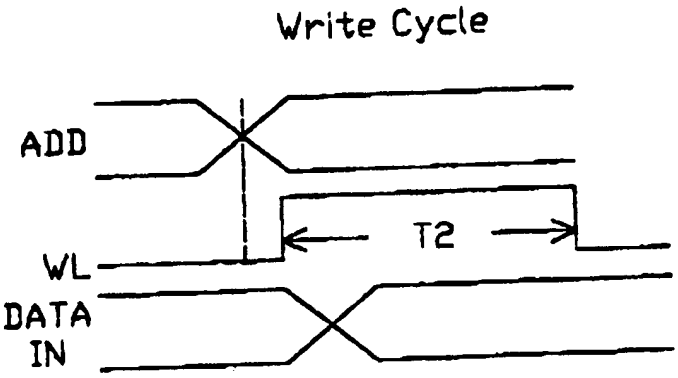
第四圖A及第四圖B藉由電路信號的時序圖，說明本發明的技術特點。



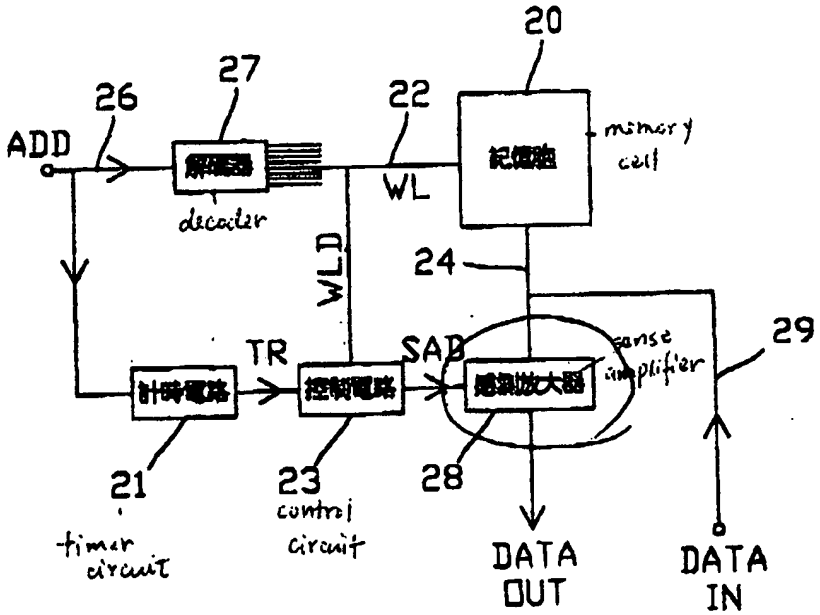
第一圖 Prior Art



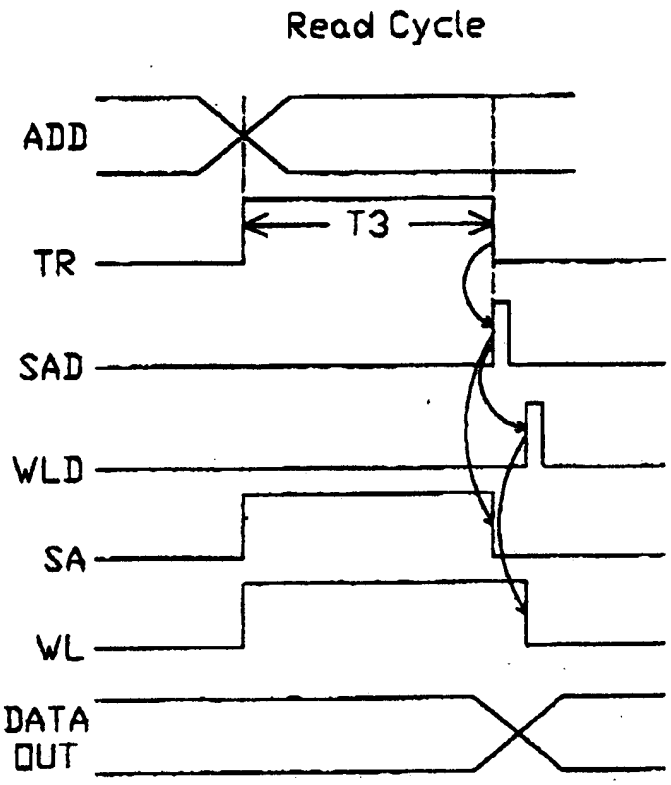
第二圖 A Prior Art



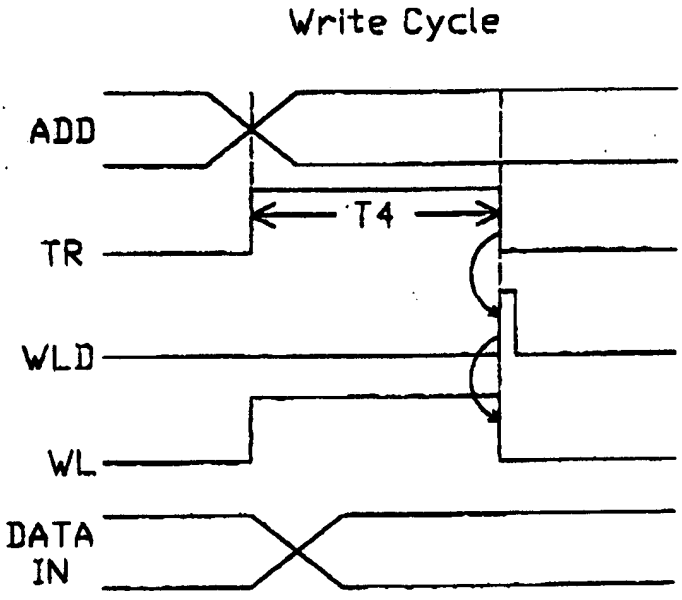
第二圖 B Prior Art



第三圖


Read Cycle
ADD
T3
TR
SAD
WLD
SA
WL
DATA
OUT

第四圖 A


Write Cycle
ADD
T4
TR
WLD
WL
DATA
IN

第四圖 B

(ENGLISH TRANSLATION)

FIRST OFFICE ACTION

Date of Receipt: June 17, 2004

1. APPLICATION NO.: 91136565
2. TITLE: Power reduction in a memory bus interface
3. APPLICANTS: Intel Corporation
   ADDRESS: U.S.A.
4. ATTORNEY: Patrick I. C. Yun/William W. L. Chen
5. FILING DATE: December 18, 2002
6. PRIORITY DATA: U.S. application serial no. 10/038,960 filed 2002/01/02
7. CONTENTS OF ACTION:

SUBJECT

The invention in this application shall not be granted an Invention Patent on the basis of the provisions in Article 20.2 of the Patent Law.

REASONS

1. The invention in this patent application entitled, "Power reduction in a memory bus interface," relates to a technique which includes amplifying data signals from a memory bus interface (16). The amplified data signals are sampled, and the amplifying function of the amplifier is selectively turned off within certain selected period. That is, the amplification may be selectively enabled in response to the beginning of the predetermined operation over the memory bus.

2. This invention, by means of certain logic gate control circuit, turns off the amplifying action of the amplifier in response to the absence of a predetermined operation occurring over the memory bus, and has reduced the electrical power consumed by the amplifier circuit. It is noted that, from among the relevant local and foreign references prior to the filing date of this invention, Taiwanese patent publication no. 459242 (see attached cited reference), which was published October 11, 2001, has disclosed the above-described technique. The present invention made an adaptation within a similar or closely related technical field but failed to produce any outstanding feature or a distinct improvement. Therefore, such an adaptation is regarded to be easily achievable by one skilled in the art. This invention made substitution and variation in the arrangement and combination of the constituted elements of the cited reference but failed to produce any outstanding feature or a distinct improvement. Therefore, this invention utilizes technology or knowledge in existence prior to its filing and can be easily accomplished by those skilled in the art and, hence, this invention is devoid of inventive step.

In view of the aforesaid, the invention in this application is in contravention of the provisions in Article 20.2 of the Patent Law and accordingly shall not be granted an Invention Patent.

Sealed By
Lian-Sheng Tsai
Director

NOTE: If dissatisfied with this Office Action, the Applicant may file a request for reexamination along with a Response within thirty (30) days of the day following the date of receipt of this Office Action.